Readout and Control System Requirements

BTeV Document (number to be assigned)

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1 Introduction

This document describes the highest level requirements for the BTeV Readout and Control System. The purpose of the BTeV Readout and Control System is to transfer detector data to archival storage, interfacing with the various triggering components as needed. This system also includes the monitoring and controls of the detector itself.

2 High Level Requirements

This section describes Readout and Control System requirements that are necessary to achieve the goals of the BTeV experiment. Note that "event" in this document refers to data from a single crossing, regardless of the number of interactions in the crossing.

2.1 Input Rate Requirements

Most of the data produced by the detector is below predetermined thresholds and is suppressed at the detector. Approximately 10^{13} bits per second leave the detector and must be processed by the Readout System. The Readout System may provide compression for data that has not already been compressed at the detector. All data presented to the Readout System Electronics is expected to be in digital form.

- **Requirement 2.1-1 (Input data rate):** The BTeV Readout System must accept a data rate of at least 10^{13} bits per second.

2.2 Intermediate Rate Requirements

The combined acceptance of the first level trigger is expected to be approximately 1% of all crossings. The data size of these accepted events may be larger than the average for all events, and additional data will be generated by the first level triggers.

- **Requirement 2.2-1 (First level buffering):** The Readout System must buffer all data received from the detector for the period of the first level trigger decision.
- **Requirement 2.2-2 (Second level data rate):** The Readout System must be capable of delivering a data rate of 2×10^{11} bits per second (2% of the data transmitted from the detector) to the second level of the trigger system.

2.3 Output Rate Requirements

The combined acceptance of the second and third level trigger is expected to be approximately 0.05% (check this number) of all crossings. The Readout System writes data from the third level trigger system to permanent storage. Some of the output data may be summarized, resulting in a reduction in event size of at least 50%.

- **Requirement 2.3-1 (Output data rate):** The Readout System must be capable of delivering a data rate of 5×10^{9} bits per second from the third level trigger processors to the data storage system.
- **Requirement 2.3-2 (Reverse datapath):** The Readout System must be capable of delivering data at a reasonable rate from the data storage system to the processors, allowing use of the processors for offline reconstruction when the detector is not operating.

2.4 Excess Capacity & Scalability

Readout System bandwidth requirements are based on the sum of estimated data rates for each of the subdetectors.

- **Requirement 2.4-1 (Scalability):** The Readout System must permit an increase in capacity (with additional components) of at least a factor of two in data throughput at every level.

3 Readout Electronics

As the architecture for the Data Acquisition system is defined in parallel with the Level 1 trigger architecture, a implementation of multiple, parallel DA subsystems is starting to converge. Each one working on a complete event, and each one operating at 1/n the data rate, where n is the number of parallel systems. This document will refer to these parallel systems as *branches*.

3.1 Generic

The following requirements apply to all components of the Readout Electronics.

- **Requirement 3.1-1 (Control & status):** The Readout Electronics must respond to Run Control commands and must provide error and status information to the Error Handling/Recovery and Status Monitoring Systems.
- **Requirement 3.1-2 (Fault tolerance):** The Readout Electronics must continue to operate in the presence of faults, such that only data from the failed component is affected. Error detection must be sufficient to automatically identify and isolate failed components.

3.2 Data Combiners

The Readout System will provide a standard component (Data Combiner) for receipt of digital data from front-end modules. The Data Combiner will also distribute control, monitoring and timing information to/from the front-end modules.

- **Requirement 3.2-1 (Number of front-end ports):** The Data Combiner must accept data from as many front-end boards as necessary to effectively utilize the bandwidth of the output data links.
- **Requirement 3.2-2 (Processing & buffering):** The Data Combiner must be capable of performing data compression on any uncompressed data received, and must provide sufficient local buffering to smooth data rates on the output data links.
- **Requirement 3.2-3 (Remote access):** The Data Combiner must be remotely resetable and reconfigurable under all conditions not involving hardware failure of the module.
- **Requirement 3.2-4 (Timing distribution):** The Data Combiner must distribute control and synchronous timing signals, as necessary, to each front-end module.

3.3 Data Links

Data is transmitted from the detector to the counting room on short reach optical links. The Data Links are routed from the detector to the counting room through conduits with a cross sectional area of approximately 2000 square centimeters (this may place a limit on the number of fibers that can be routed).

- **Requirement 3.3-1 (Cable bandwidth):** Maximum link distance is approximately 70 meters. The cable must allow operation within the specified error rate over a distance of at least 100 meters at 2.5 Gbps or higher.
- **Requirement 3.3-2 (Error rate):** The maximum allowable bit error rate for an individual data link is 10^{-15}. This corresponds to a system bit error rate of less than 30/hr for each stage of data transmission.

- **Requirement 3.3-3 (Error detection and recovery):** The data link protocol must provide error detection and automatic resynchronization on packet boundaries.
- **Requirement 3.3-4 (Synchronization):** Serial data links must be synchronized to local oscillators (not to the accelerator clock).

3.4 First Level Buffers

The First Level Buffers receive data from the Data Combiners and various stages of the First Level Trigger. The data is held until a trigger decision is made, and then either discarded or forwarded to the Second Level Trigger.

- **Requirement 3.4-1 (Buffer size):** The First Level Buffers must be capable of holding data until a first level trigger decision is made. It is assumed that the decision time will be limited by a timeout in the first level trigger.
- **Requirement 3.4-2 (Input data ordering & format):** The First Level Buffers must accept data that is not in crossing order, but may impose a requirement on sources that all data be **grouped** by crossing (i.e., data from crossing n may arrive either before OR after data from crossing m, but may not arrive both before AND after.) The First Level Buffers must extract framing information (crossing number and end-of-record) from received data packets for use in identifying and routing the data.

3.5 Event Builder

For each event accepted by the first level trigger system, all necessary data from all detector subsystems must be combined and delivered to processors in the second level trigger system.

- **Requirement 3.5-1 (Data rate):** The Event Builder must be capable of delivering a combined rate of 2×10^{11} bits per second to the second level trigger system.
- **Requirement 3.5-2 (Data routing):** The Event Builder must be capable of routing data from any first level buffer to any second level trigger processor within a branch.
- **Requirement 3.5-3 (Data buffering):** The Event Builder must hold data received from the first level buffers for a complete event until it has been delivered to the second level trigger.
- **Requirement 3.5-3 (Trigger Tables):** Calculated data on L1 trigger decisions must input to which partition data are routed.
- **Do we need to simulate L1 in software for commissioning?**

3.6 Timing

The Timing system generates signals that are synchronous to the accelerator clock. It is assumed that only the Data Combiners and associated front-end electronics will require synchronous timing, and that all other components of the Readout System and Trigger System operate asynchronously. The clock signal will likely be 53 or 106 MHz. Alignment of the 7.6 MHz (132 nsec) crossing clock will be provided by a synchronous command signal.

- **Requirement 3.6-1 (Synchronous clock):** The Timing System must provide a clock which is synchronized to the accelerator RF (53.104 MHz), and must distribute this clock independently to all Data Combiners. The synchronous clock must have no more than xxx psec of jitter.
- **Requirement 3.6-2 (Command synchronization):** The Timing system must deliver at least one synchronous signal for the purpose of aligning commands to specific clock edges. Commands may be delivered asynchronously or may be implied.

3.7 Gating and Control Distribution

Each subsystem has a local manager which communicates with Run Control and directs the operation of components in that subsystem. The manager consists of a standard processor and associated software, along with the electronics necessary to distribute synchronous and asynchronous control signals within the subsystem.

- **Requirement 3.7-1 (Synchronous control distribution):** The control signal distribution electronics for the Detector Managers must drive independent synchronous links to each Data Combiner. The distribution electronics must provide global timing alignment for each detector and must add no more than xxx psec of jitter to any signal. The distribution point for Data Combiners must be outside the collision hall.
- **Requirement 3.7-2 (Asynchronous control distribution):** The control signal distribution electronics for all managers must provide bidirectional links for asynchronous control and monitoring of each component in the subsystem. The distribution point for Data Combiners must be outside the collision hall.

3.8 Firmware

Components of the Readout Electronics will include embedded software in the form of FPGA firmware and microcontroller code. The embedded software should comply with the standards defined in the *BTeV Software Standards* document wherever possible. This code will be developed using application specific tools including compilers, debuggers, and diagnostics.

- **Requirement 3.8-1 (Software repository):** All firmware (source and object code) must reside in a software repository that will be used to keep track of different versions of the firmware as it is being developed.
- **Requirement 3.8-2 (Version control):** The version number of the firmware that is used to process data must be managed in such a way that the firmware version that was used to process data can always be identified.
- **Requirement 3.8-3 (System Software error detection):** Processes to regularly verify code and run standard datasets must be included.
- **Requirement 3.8-4 (Development tools archival):** The development software and operating environment necessary to recreate the last implemented version of firmware for each component must be archived. Any unique hardware platforms or keys used in the firmware development process must also be identified and tracked.

3.9 Electronics Standards

The hardware that is designed and built, or purchased to implement the readout system will consist of digital electronics. This hardware must comply with the *BTeV Digital Electronics Standards* document. This document contains requirements, standards, and recommendations that apply to all digital electronics in BTeV. The subjects that are addressed in the document include interfaces, grounding, EMI, shielding, infrastructure, safety, reliability, and maintainability.

- **Requirement 3.9-1 (Electronics standards):** The readout system must comply with the *BTeV Digital Electronics Standards* document.

3.10 Reliability

- **Requirement 3.10-1 (Burn-in):** The Readout System hardware must undergo a burn-in process to minimize infant mortality failures in the production system.
- **Requirement 3.10-2 (Low-stress design):** Circuit board assembly techniques must be employed to minimize component stress that would adversely affect reliability.
- **Requirement 3.10-3 (Fault tolerance):** A level of fault-tolerance and redundancy must be designed into the architecture so that a noticeable percentage of processing elements must fail before the normal operation of the system is significantly affected.
- **Requirement 3.10-4 (Uptime):** The Readout System must be ready to run during 95% of beam time (no more than 5% dead time for initialization, startup, etc.)

3.11 Test Features

The subsections below contain requirements pertaining to the testability of the Readout System components.

- **Requirement 3.11-1 (Self-test):** Components must include built-in test structures such that all internal functions of the module may be tested with minimal use of external test equipment.
- **Requirement 3.11-2 (Interface test):** Components must include built-in pattern generation and checking such that the interfaces to upstream and downstream components may be tested with minimal use of external test equipment.

3.12 Maintainability

- **Requirement 3.12-1 (Maintenance):** Sufficient numbers of spares must be assembled to allow the Readout System to be maintained by module replacement.
- **Requirement 3.12-2 (Modularity):** The size and complexity of individual circuit boards must be minimized, such that replacement of a board can be considered a viable option to repair.
- **Requirement 3.12-3 (Programming):** All programmable components must be "in-circuit" reprogrammable. If there is no permanent data link to the component, the programming interface must be accessible without removing the component from the system.

3.13 Module and Link Identification

All electronics modules and links require identification.

- **Requirement 3.13-1 (Module identification):** Each electronics module must have a label containing a unique bar code and its alphanumeric equivalent. Any module with a control system connection must also be identifiable by a unique electronic tag, which may be a network address.
- **Requirement 3.13-1 (Link identification):** Each data link must have a label containing a unique bar code and its alphanumeric equivalent. Any link longer than 2 meters, or not fully visible when installed must be labeled at both ends. Shorter cables too?

4 Controls and Software

Higher level software is required for running and monitoring the experiment. This includes run management software, detector monitoring software, partitioning of the readout and controls resources as well as the detector itself, and data storage. This services will be provided in a distributed environment which needs to communicate with the other sub system managers.

4.1 Generic

- **Requirement 4.1-1 (Standards):** All software that is designed, or purchased to implement the system control functions must comply with the *BTeV Software Standards* document.
- **Requirement 4.1-2 (Deadtime):** Software infrastructure cannot introduce more than %x deadtime into the readout. (0.5?). How long are runs, how often does one redownload?

4.2 Run Management

Run Management software is necessary for starting/stopping and organizing all components for data taking.

- **Requirement 4.2-1 (Hierarchy):** The Run Management software must provide a central facility for system start, stop and automatic error recovery.
- **Requirement 4.2-2 (Performance monitoring):** The Run Management software must provide appropriate monitoring/diagnostic information on DA performance for shift personnel through data taking periods.
- **Requirement 4.2-3 (Information Services):** The Run Management software must archive run conditions for viewing offline.
- **Requirement 4.2-4 (Error recovery):** Run Management software must provide central facility to process various component failures and to provide automated mechanisms for recovery where possible.
- **Requirement 4.2-5 (Configuration changes):** Run management software must provide interface to change and track changes to run parameters.
- **Requirement 4.2-6 (Partitioning):** Run management software must support multiple, independent runs. **Requirement**
- **Requirement 4.2-7 (Remote Access):** Remote monitoring and configuration must be supported during normal operating conditions.
- **Requirement 4.2-8 (Multi-platform support):** User interfaces must operate across a variety of operating system platforms.
- **Requirement 4.2-9 (Connectivity):** The Run Control Host must have access (through the control network) to all other subsystem managers/controllers in the system.
- **Requirement 4.2-10 (Reliability): –** How to address single points of failure (run control host …)
- **Requirement 4.2.11 (Performance):** - Run starts during the commissioning phase must be tunable to have minimal overhead times.

4.3 Buffer Manager

The Buffer Manager is the central point for assignment of events to second level trigger processors. It receives trigger decisions from the First Level Trigger System and receives requests for events from the

Second Level Trigger System. It is also the central point for download and initialization of Readout System components.

The Buffer Manager may reject events which have passed the first level trigger if there are no pending requests from the second level trigger system, or if buffers in the Readout System datapath have reached an almost full condition. Alternately, the Buffer Manager may provide an inhibit signal to the first level trigger under these conditions, with the expectation that only reject decisions will be returned while the inhibit signal is asserted.. The Buffer Manager may also automatically reject events if no decision has been received from the first level trigger within a specified timeout period.

- **Requirement 4.3-1 (Assignment rate):** The Buffer manager must be capable of assigning events to second level trigger processors at an average rate of 100,000 events per second.
- **Requirement 4.3-2 (Level 1 accepts):** The Buffer manager must assign all events accepted by the first level trigger which do not exceed the bandwidth, buffer or processing resource limitations of the Readout System or second level trigger system, and must deliver these assignments to all first level buffers.
- **Requirement 4.3-3 (Statistics):** The Buffer Manager must keep statistics on the number of events rejected for reasons other than first level trigger decisions.
- **Requirement 4.3.4 (Interfaces)**: Must conform to data acquisition software and control environment standards. (run control client, status and error reporting, etc).

4.4 Trigger Managers

The first and second level Trigger Managers are currently viewed as part of the Trigger subsystems. However, they perform the same function as other subsystem managers and may benefit from a common implementation.

4.5 Detector Manager

The Detector Manager provides control/monitor fan-out and fan-in for the Data Combiners associated with a specific subdetector. It also allows standalone local control and monitoring of the subdetector. The Detector Managers may be implemented using the same basic hardware and software for all subdetectors, but may also include detector-specific software.

The Detector Manager receives and processes all control messages from the Run Control system and returns status information. It also controls the interface between the general timing system and individual subdetector Data Combiners.

- **Requirement 4.5-1 (Function):** The Detector Manager must allow standalone operation of a complete subdetector. This includes control and monitoring of both Run Control and Slow Control functions and emulation of synchronous signals from the Timing system. It must also be capable of reading (at a significantly reduced rate) any data which would normally be transmitted over the Readout System data links.
- **Requirement 4.5-2 (Alarms):** The Detector Manager must be capable of locally displaying all subdetector alarms, in addition to passing this information to the Slow Control Host.

4.6 Partitioning

During commissioning phases of both the detector and components of the L1 and L2/L3 processing farms, multiple runs will need to happen in parallel using a different set of resources. Some resources, may however, be shared (data switches, the global level 1 trigger, etc.). Partitioning is the ability to provide

concurrent, independent runs with their own user defined trigger requirements and user defined resources. Partitioning must support more than just hardware commissioning - one may split trigger processing nodes into different partitions to test different algorithms or OS versions, etc.

- **Requirement 4.6-1 (Granularity):** Must be able to commission sub-detectors without relying on other sub-detectors to be operational.
- **Requirement 4.6-2 (Heterogenous)** Must support ability to have different trigger algorithms in the same partition
- **Requirement 4.6-3 (Maximum size):** A single partition must be able to support the entire BTeV detector (ie, normal running).
- **Requirement 4.6.4 (Resource Ownership):** Resources must be only be reserved for write access by a maximum of one partition. The granularity of a resource should be the smallest unit that does not impact other resources. Not all of a resource needs to be functional for it to be included in a partition
- **Requirement 4.6-5 (Shared resources):** Resources must be capable of being shared across partitions.
- **Requirement 4.6-6 (Communication):** All affected partitions must be notified when shared resources are modified.
- **Requirement 4.6-7 (Excess Resources):** Idle L3 processing nodes must be available for use outside the data acquisition system.
- **Requirement 4.6-8 (Routing)** Data from any crossing must be able to go to any partition (ie, a given partition can receive consecutive crossings).
- **Requirement 4.6-9 ()** Data from a particular beam crossing must go to all partitions that satisfy its trigger requirements.
- **Requirement 4.6-10 ()** A given partition will receive a specific beam crossing no more than once.
- **Requirement 4.6-11 (Excess Capacity)** Idle L3 processing nodes must be available outside the data acquisition system.

4.7 Data Storage

Events passing the second and third level triggers will be transmitted via optical links to a permanent storage system located in the Feynman Computing Center.

- **Requirement 4.7-1 (Storage system bandwidth):** The storage system must accept an average data rate of 2 X 10^9 bits per second.
- **Requirement 4.7-2 (Shared Resources):** The storage system must use the same archival robotics and media as BTeV offline.
- **Requirement 4.7-3 (Buffering):** If the second level processors have local attached disk drives, these may be used to buffer data during short power or network interruptions at Feynman. The network supplying data to the data storage system and the data storage system itself must have excess bandwidth capacity to offload this accumulated data in a reasonable period of time.
- **Requirement 4.7-3 (Streaming):** Data storage must support storing similar events based on trigger type as a collection**.**
- **Requirement 4.7-4 (Duplication of data).** Some data must be routed to more than 1 stream.

4.8 Slow Control

The BTeV Slow Control system is used to monitor and set control/alarms on the detector and in the off-detector electronics (pressures, temperatures, high voltages, etc.)

- **Requirement 4.8-1 (Segregation):** The Slow Control system must provide a data path which is independent of the Readout System data path, and/or must remain operational when the Readout System is off-line.
- **Requirement 4.8-2 (Archival):** Slow control data and alarms must be archived at a rate appropriate to the functions being monitored, such that the state of the system is fully defined for later analysis in the offline code.
- **Requirement 4.8-3 (Alarms):** The Slow Control Host must provide a centralized alarm display for all subsystems.
- **Do error s here need to stop data taking or inhibit it from starting?**

5 Infrastructure and Integration

5.1 Control Network

The Control Network provides a general-purpose interconnection for all other subsystems in the BTeV experiment. Run control commands need to be routed to components both in parallel and in series.

- **Requirement 5.1-1 (Control Network bandwidth):** The Control Network must provide sufficient bandwidth for efficient database access, download, monitoring, slow control and run control functions.
- **Requirement 5.1-1 (Interconnection):** The control network must support a broadcast capability.

5.2 Control Room

The Control Room…

- **Requirement 5.2-1 (Accessiblity):** All information must be electronically accessible

5.3 Databases

Databases are used throughout the system to provide accesses to configuration parameter and to log status information. There may be several global databases as well as local databases associated with each subsystem.

- **Requirement 5.3-1 (Uptime):**
- **Requirement 5.3-2 (Backups/recovery)**
- **Requirement 5.3-3 (Platform Accessibility)**
- **Requirement 5-3.4 (Reliability)**
- **Requirement 5-3.5 (Performance)**
- **Requirement 5-3.6 (Scalability)**

- **Requirement 5-3.7 (Longevity): Data must be available for n years after data taking has stopped.**
- **Requirement 5-3.8 ():** Some online database information must be shared and synchronized (both directions) with data in offline databases.

5.4 Test Stands

To the extent possible, all BTeV electronics will include built-in self-test features. "Test stands" for these individual components will consist mainly of a small power source and a means of connecting the component to a standard desktop PC. For larger system tests, a test stand which simulates the actual operating environment (full system rack) will be necessary. An attempt will be made to minimize the number of components designed solely for test purposes.

- **Requirement 5.4-1 (Component test stands):** A standard development/test system including user modifiable, application-specific software and benchtop power must be provided for testing of individual electronics components.
- **Requirement 5.4-2 (System test stands):** A standard rack based development/test system including system level software and power must be provided for testing of multiple components in a system environment.

5.5 Installation

Installation…

- **Requirement 5.5-1 ():** The

6 Safety and Computer Security

6.1 Safety

The Readout and Control System does not pose safety concerns beyond the usual and customary issues associated with high-current low-voltage digital electronics:

- **Requirement 6.1-1 (Low Voltage, High Current Safety):** If high-current (greater than 10 amps operating or 50 amps rated current), low-voltage (less than 50 volts) supplies power the digital circuitry, the safety requirements for high current power distribution systems must be followed. These are detailed in the Fermilab ES&H Manual, Occupational Safety And Health section on Electrical Safety which can be accessed at www-esh.fnal.gov/FESHM/5000/5046.html.
  Also, a hazard analysis sheet must be completed and signed by any person who will be working with any low-voltage, high-current system, circuit board, or other electronic device. The internal wiring of a commercially manufactured piece of equipment is exempt as detailed in the FESHM section reference above. The reference provides guidance on load connections, ribbon cables, multiple conductors and mechanical components.
- **Requirement 6.1-2 (Computers): Safety of people or equipment cannot rely on computers or software.**

6.2 Security

- **Requirement 6.2-1 (Standards):** BteV readout and control system must conform to the Fermilab Computer Security Protection Plan

- **Requirement 6.2-2 (Isolation):** Readout and controls system must operate when cut off from the Fermilab network.
- **Requirement 6.2-3 (Rate):** Network architecture must be such as to allow for rapid isolation from the rest of the Fermilab network.

Dependency Appendices

A. Detector and Front-end Electronics Dependencies

A.1 Front-end to Data Combiner

- **Dependency A.1-1 (Input data):** All data presented to the Readout System Data Combiners must be in digital form. To minimize the number of different Data Combiner designs, an optional front-end to Data Combiner Link specification will be proposed. Subsystems which adhere to this specification may interchange Data Combiner modules.

A.2 Detector Data Rates

Cost and scaling of the Readout System is directly proportional to the expected volume of data from the detectors. We rely on a reasonably accurate prediction of average and worst-case data rates from each subdetector.

- **Dependency A.2-1 (Predicted data rates):** The bandwidth requirements of the Readout System will be based on the estimates of data rates provided by each subdetector, with some additional margin. These estimates should be as accurate as possible.

A.3 Detector Timing

The Timing system and Data Combiners will distribute clock and synchronous command signals to front-end electronics as necessary. There are several options for distribution of these timing signals, but most will require that fine adjustments (less than one clock period at 53 MHz) be done at the front-end module. The Timing system will maintain a maximum jitter specification but will only correct for phase differences in increments of one clock period. The front-end electronics must compensate for differences in cable lengths and other delays following the Data Combiners.

- **Dependency A.3-1 (Timing signals):** Subsystems requiring synchronous signals with better than +/- 10 nsec phase resolution must provide local timing adjustment.

A.4 Slow Control

- **Dependency A.4-1 (Interface):** Interface to the main BTeV slow control system must be through a common SCADA package.

B. First Level Trigger Dependencies

B.1 Trigger Latency

The **average** latency for first level trigger decisions cannot exceed the time needed to fill a first level buffer at the maximum input data rate. Also, assuming the use of DRAM in the buffer implementation, it is preferred that the **maximum** latency of the first level trigger decision not exceed 50 milliseconds, so that buffer memory refresh operations are not necessary.

- **Dependency B.1-1 (Latency):** The first level trigger must return a decision for all crossings within a specified maximum latency, even if processing for those crossings is not complete.

B.2 Trigger Data Format

Data from the first level trigger may be stored in first level buffers at various stages of the trigger calculation. The input bandwidth of the first level buffers is dependent on the format of data received. The buffers expect to receive data which has been grouped by timestamp (crossing number), so that transfers to and from the memory can be performed in blocks. If the received data is not grouped, the buffer input bandwidth may decrease by a factor of 10 or more.

- **Dependency B.2-1 ( ):** The first level trigger must group data written into First Level Buffers so that all data from a specific crossing in contiguous.

C. Second Level Trigger Dependencies

C.1 Request Timing

There may be a significant latency (many milliseconds) between the time a request for a new event is issued by a second level trigger processor and the time that the event data is delivered to the processor. To avoid idle time, processors should issue requests well in advance.

- **Dependency C.1-1 (Latency):** Each processor in the second level trigger must request in advance and be capable of buffering returned data from as many events as necessary to avoid excess idle time waiting for data.
-

D. Facilities Dependencies

D.1 Installation

There are minimum space and power requirements for the readout and control electronics.

- **Dependency D.1-1 (Collision hall):** The Readout and Control electronics located in the collision Hall will require xxxU of rack space, xxx watts of electrical power and xxx BTU/hr of heat removal.
- **Dependency D.1-1 (Counting room/Control room):** The Readout and Control electronics located in the counting Room will require xxxU of rack space, xxx watts of electrical power and xxx BTU/hr of heat removal.